

## Overview

Aizyc 10/100 Ethernet MAC IP supports Fast Ethernet (10/100 Mbits/sec), as per IEEE 802.3 standards. It is best suited for SOC applications like industrial automation, switching, routing and server adapters cards.

TCP Offload Engine (TOE) is implemented in this IP to make it most suitable for high speed networks. This engine will offload TCP/IP/UDP protocol processing like segmentation and TCP/IP/UDP checksum calculation.

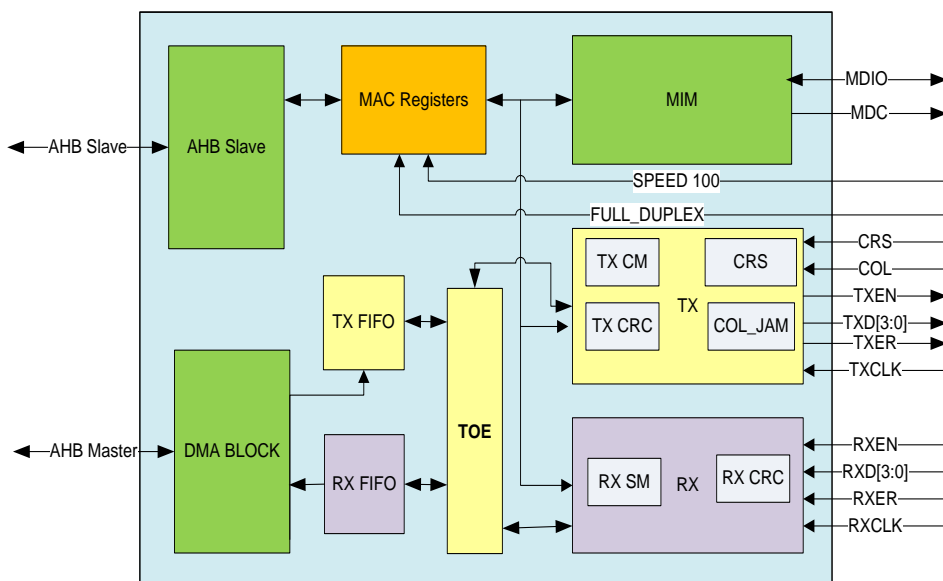
IP provides standard interface - IEEE 802.3 Media Independent Interface (MII) with optional support for Reduced Media Independent Interface (RMII). For management and control functions, MDIO (Management Data Input/Output) and MDC (Management Data Clock) interface is provided.

Software Solution to support EtherCAT and Profinet is available along with hardware accelerators. IP is available with AHB interface for easy compatibility, with optional OPB or OCP Interface support. IP provides two separate configurable FIFOs for transmit and receive.

IP Supports full implementation of Carrier Sense Multiple Access with Collision Detection (CSMA/CD). IP supports configurable Inter Frame Gap, automatic padding of short frame and automatic detection of excessive short and long packets. IP has simple DMA for receive and transmit data path.

The IP core is portable to either an ASIC or a FPGA. It has been validated on Xilinx Spartan 3 platform. Along with the IP core, we will also provide complete test environment with constraint randomized test cases. Our full support will be available to help you in complete integration.

## Functional Block Diagram



## 10/100 Ethernet MAC IP

### Features

- Compliant with standards IEEE 802.3-2002
- Host Interface : AHB, Optional : OPB , OCP
- Network Interface : MII (Optional RMII)
- Management Interface : MDIO/MDC
- Implementation for TCP Offload Engine (TOE)
- Supported frames:
  - Magic packet
  - Wake up frames
  - VLAN Frame
- CSMA/CD Protocol for Half-duplex Mode
- One 48 bit perfect address
- Flexible address filtering modes
- Support to all Multicast addresses
- 64 hash filtered multicast addresses
- Preamble generation of variable length (3,5,7 bytes)
- Automatic padding of short frame
- Automatic detection of excessive long and short packets
- Programmable Inter Frame Gap
- FCS transmission and reception
- Supports Promiscuous Mode
- Simple DMA for Receive and Transmit
- Configurable depth transmit and receive FIFOs
- Transmit and Receive Statistics Vector
- Full duplex control using PAUSE frame generation and detection
- CRC 32 - CRC generation and checking

## Functional Block Description

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### MIIM

This block performs PHY management registers read and write operations through MDIO/MDC interface. The PHY address and register address have to be programmed in MAC Registers before this block accesses the PHY.

### TX Controller

Transmit controller block control the data transmission operation. These operations include preamble insertion, pad bytes, FCS calculation and insertion, SFD, collision Detection and retransmission of packets

### RX Controller

Receive controller is responsible for detection and checking of received packets. This block drops all the malformed packets such as packets with wrong SFD, destination address and FCS. Only valid packets are stored into the RX buffer.

### MAC Registers

This block contains all of MAC IP control and status registers.

### DMA Block

The DMA block transfers data from system memory to TX buffer and from RX buffer to system memory. This block generates interrupt when a packet is transmitted or when a packet is received and transferred to Main memory

### TCP/IP Offload

The offloading of TCP/IP/UDP protocol processing is done by the TCP/IP/UDP offload Engine (TOE). The main function Of TOE is segmentation, TCP/IP/UDP checksum calculation and update respective fields in the header of the packet.

### TX/RX FIFO

The IP consists of configurable 4K bytes TX and 2K bytes RX 2-port buffers. These buffers act as bridge between TX/RX Controllers and DMA engine.

### AHB Interface

A 32-bit AHB slave interface is provided as configuration interface for write and read to MAC registers. A 64-bit AHB Master interface is provided to transfer data to/from the system memory.

## Contact Information

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## Aizyc Advantage

- Scalable IP Core
- Compact Design
- Cost-effective
- Portability : ASIC, FPGA
- Validation on Xilinx
- Continuous support during integration, design and verification

## Design Attributes

- Fully Synchronous Design
- Synchronous Reset
- No Internal tri-states
- Technology independent design
- Highly modular design
- Platforms : Solaris and Linux
- Verilog Simulators : Cadence NC-Verilog and Synopsys VCS

## Deliverables

- Synthesizable Verilog RTL
- Test bench and exhaustive Test cases
- Synthesis constraints and script files
- Sample AHB Slave Driver
- Documentation – User Manual, Verification plan , Validation Report, Synthesis, DFT and Integration Guidelines