

Overview

Aizyc SD/SDIO/eMMC Host Controller IP is compact, low power and highly configurable IP core. It is easy to integrate and very cost effective.

IP is fully compliant with the standard SD Host Controller Specifications Version 3.0, SDIO Specifications Version 3.00 and SD physical Layer Specifications Version 3.01.

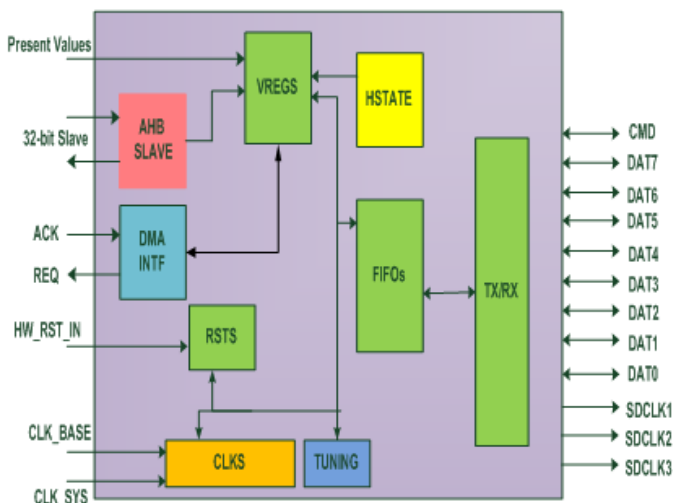
SD/SDIO/eMMC host controller IP uses a 32-bit AHB slave interface to connect to Host system and standard CARD interface on the device side. It uses a parallel interface to load preset values which can be integrated with flash device or EEPROM to define configuration specific to implementation.

This IP also provides support for eMMC 4.41 card interface.

The IP core is portable to either an ASIC or a FPGA. It has been validated on Xilinx Spartan 3 platform.

Along with the IP core, we will also provide complete test environment with constraint randomized test cases. Our full support will be available to help you in complete integration.

Functional Block Diagram



SD/SDIO/eMMC Host Controller IP

Features

- Compliant to SD Host Controller Specifications version 3.00
- Compliant to SDIO specifications version 3.00 draft 1.01
- Conforms to SD Physical Layer Specifications version 3.01
- support to eMMC4.41 interface
- System Interface – AHB
- Optional Interface – VCI, OCP, AXI, APB
- Supports SDR25, SDR50, SDR104 and DDR50 modes of operation
- Supports up to 104MBps speed
- In-built clock divider
- Assumes external PLL for implementations that choose to use multiplier for greater accuracy of clock frequency
- Configurable FIFO depth
- Supports shared SD bus to connect up to 3 devices
- Supports 1.8V, 3.3V and 3.0V operation. Chip pads are 1.8V. Board level solution is required to support 3.3V and it is controlled by a GPIO pin
- Supports Interrupt
- Supports stop at block gap
- Supports 32-bit AHB slave interface for register configuration and data transfer
- AHB slave interface supports INCR and FIXED address bursts
- Supports DMA channel Req/Ack to integrate with external DMA

Functional Block Description

DMA INTF

This block requests for DMA channel by asserting DMA_REQ to external DMA. DMA_REQ is asserted when host SW programs the IP to send a command which involves data transfer. The channel request is de-asserted when external DMA asserts DMA_ACK after completion of DMA transfer. The DMA transfer can be from system memory to the internal FIFO in the IP or vice versa.

HSTATE

Host state handles logic to determine present state of Host. It includes operations of card detection / removal, debouncing detect signal, tracking of read / write active phases, tracking DAT/CMD line busy/idle phase. It generates signals required for interrupts associated with these phases and to update present status register.

AHB Slave

The AHB slave block is used to access the SD registers by the host CPU. It operates at AHB clock frequency and the all the signals to/from this block are synchronized in SD clock domain. AHB slave interface supports FIXED and INCR address burst read/write commands.

FIFO controller

This block has 2 two port RAMS one for write transactions and one for read transaction and FIFO logic to maintain pointers. Write clock of RAM used for write transactions is clk_app and read clock is sdclk. Write clock of RAM used for read transactions is sdclk and read clock is clk_app. For DMA data write transfers, DMA writes data into the buffer and tx_rx controllers reads the data from the buffer. For DMA data read transfers, tx_rx controller writes data into the buffer and DMA reads the data from the buffer. For Non-DMA data write transfers, registers block writes data to the buffer and tx_rx controller read the data from the buffer. For Non-DMA data read transfers, tx_rx controller writes data into the buffer and register block reads the data from the buffer.

TXRX

It interfaces to CMDS and transfers data across the CARD interface serially or on 4-bit/8-bit data bus. It performs (1) CRC (2) start/stop bit insertion (3) serial-to-parallel and parallel-to-serial (4) timeout detection (5) busy detection

Design Attributes

- Fully Synchronous Design
- Technology independent design
- Highly modular design
- Platforms : Solaris and Linux
- Verilog Simulators : Cadence NC-Verilog and Synopsys VCS

Aizyc Advantage

- Scalable IP Core
- Compact Design
- Cost-effective
- Portability : ASIC, FPGA
- Validation on Xilinx
- Continuous support during integration, design and verification

Deliverables

- Synthesizable Verilog RTL
- Test bench and exhaustive Test cases
- Synthesis constraints and script files
- Sample AHB Slave Driver
- Documentation – User Manual, Verification plan , Validation Report, Synthesis, DFT and integration Guidelines



VREGS

Implements register set and interrupts

TUNING

Performs clock tuning when operating in 208MHz (and also for SDR50 if required and enabled by system). It works under software control. When enabled, it tracks data returned by device in response to CMD19, selects sampling points iteratively and picks the right sampling point for data transfer

Host State

Implements card insert/removal detection and associated functions.

Resets

Generates resets based on power on reset and software reset bits. There are two versions of synchronously released asynchronous reset those with `_sd` in the name are released synchronous to `clk_sd` resets with `_sys` in their names are released synchronous to `clk_sys`

Clocks

Clocks block generates SDCLK derived from a base clock, `clk_base`. It implements clock divider to be able to divide the `clk_base` with any even number from 2 to 2046. When clock multiplier is desired, it expects an external PLL to perform M/N and feed input as `clk_pll`. It implements clock gating for low power operation in suspend mode and when card is not present

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