

Overview

Aizyc SD/SDIO 3.0 Host IP is compact, low power and highly configurable IP core. It is easy to integrate and a very cost effective.

IP is fully compliant with the standard SD Host Controller Specifications Version 3.0, SDIO Specifications Version 3.00 and SD physical Layer Specifications Version 3.01.

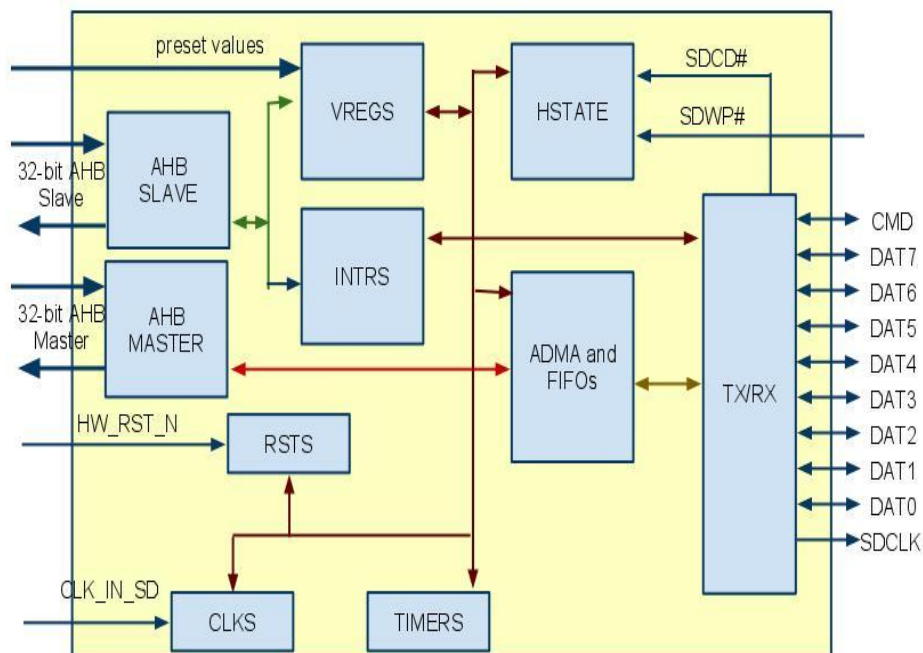
Aizyc SD/SDIO 3.0 Host IP provides supports for various system interfaces – VCI, AHB, APB and OCP. Number of slots[1/2] available is also configurable. It provides UHS-I modes of operation - DS, HS, SDR12, SDR25, SDR50, SDR104 and DDR50.

This IP also provides optional support for eMMC 4.41 card interface.

The IP core is portable to either an ASIC or a FPGA. It has been validated on Xilinx Spartan 3 platform.

Along with the IP core, we will also provide complete test environment with constraint randomized test cases. Our full support will be available to help you in complete integration.

Functional Block Diagram



SD/SDIO 3.0 – Host Controller IP

Features

- Compliant to SD Host Controller Specifications version 3.00
- Compliant to SDIO specifications version 3.00 draft 1.01
- Conforms to SD Physical Layer Specifications version 3.01
- Optional support to eMMC4.41 interface
- System Interface – AHB
- Optional Interface – VCI, OCP, AXI, APB
- Supports following UHS-I modes of operation
 - DS – Default speed mode up to 25MHz 3.3V signalling
 - HS – High Speed mode up to 50MHz 3.3V signalling
 - SDR12 – SDR up to 25MHz 1.8V signalling
 - SDR25 – SDR up to 50MHz 1.8V signalling
 - SDR50 – SDR up to 100MHz 1.8V signalling
 - SDR104 – SDR up to 208MHz 1.8V signalling
 - DDR50 – DDR up to 50MHz 1.8V signalling
- Supports SPI, 1-bit and 4-bit SD modes
- Supports single slot. Option to support multiple slots
- Supports clock tuning
- In-built clock divider
- Support CRC7 and CRC16 generation/checking
- Supports IO52 and IO53 commands for SDIO cards
- Supports Read Wait Control and Suspend/Resume operations
- Supports SDMA and ADMA
- Configurable FIFO depths
- Supports stop at block gap
- Support interrupt
- Supports 1.8V, 3.3V and 3.0V operation. Chip pads are 1.8V. Board level solution is required to support 3.3V and it is controlled by a GPIO pin

Functional Block Description

VREGS

VREGS implements majority of registers of the chip. It is interfaced over AHB slave to let the Host read / write from / to registers. It generates controls to all other blocks based on register and combinations. It outputs the register contents to configure other block. It reads status of all blocks and presents to Host on addressed registers. It works on a non stoppable system clock clk_sys_ns. Since register access must be allowed in low power states too, registers' block is run on non stoppable clock.

HSTATE

Host state handles logic to determine present state of Host. It includes operations of card detection / removal, debouncing detect signal, tracking of read / write active phases, tracking DAT/CMD line busy/idle phase. It generates signals required for interrupts associated with these phases and to update present status register.

Interrupts

This block implements interrupt registers. It receives interrupt signals from various sources and provides the status to Host through reads. It masks interrupt status based on mask registers and generates the interrupt based on interrupt status register and interrupt enable registers.

CMDS- Comand Path

Transmits and tracks commands. It also tracks response and generates controls to show the command flow. It implements command in hibit command detection. It also generates auto commands ACMD12 and ACMD23.

Clocks

Clocks block generates sd_clk derived from a base clock, clk_base. It implements clock divider to be able to divide the clk_base with any even number from 2 to 2046. When clock multiplier is desired, it expects an external PLL to perform M/N and feed input as clk_pll. It implements clock gating for low power operation in suspend mode and when card is not present.

Design Attributes

- Fully Synchronous Design
- Technology independent design
- Highly modular design
- Platforms : Solaris and Linux
- Verilog Simulators : Cadence NC-Verilog and Synopsys VCS

Aizyc Advantage

- Scalable IP Core
- Compact Design
- Cost-effective
- Portability : ASIC, FPGA
- Validation on Xilinx
- Continuous support during integration, design and verification

Deliverables

- Synthesizable Verilog RTL
- Test bench and exhaustive Test cases
- Synthesis constraints and script files
- Sample AHB Slave Driver
- Documentation – User Manual, Verification plan , Validation Report, Synthesis, DFT and integration Guidelines



LIST PROC

List processor processes the command list and performs DMA for ADMA. It also handles single block transfers for SDMA and buffer access mechanism for non DMA transfers

TXRX

It drives and samples CMD/DAT lines based on requests from LIST_PROC or CMDS. It implements CRC checks, index check, end-bit check and timeout detection.

VCI/AHB/OCP Master/Slave Interface

The 32-VCI /AHB/OCP slave interface is used to program the host registers. The 32 bit VCI/AHB/OCP master interface is used to transfer data to and from system memory.

Contact Information

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