

Overview

Aizyc SD/SDIO Device IP is compact low power and scalable IP core. It is easy to integrate and cost effective IP.

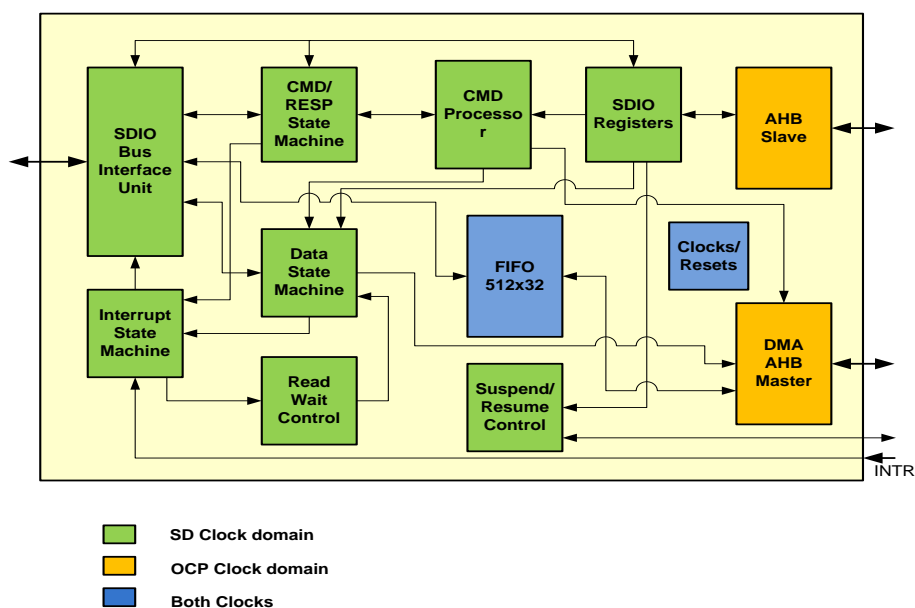
Aizyc's device IP is fully compliant with the standard SD device Controller Specifications Version 2.0, SDIO Specifications version 2.00 and SD Physical Layer Specifications Version 2.0. It supports SPI, 1-bit SD and 4-bits SD, high speed and full speed transfer modes. Data rate up to 200 Mbps in 4-bit SD mode is supported.

AHB Master & Slave interface in Host IP will allow easy integration in to SOC. The CIS and CSA have to be implemented in the internal memory of CPU subsystem.

The IP core is portable to an ASIC or a FPGA. It has been validated on Xilinx Spartan 3 platform.

Along with the IP core, we will provide complete test environment with constraint randomized test cases and our full support during integration.

Functional Block Diagram



SD/SDIO 2.0 – AHB Device IP

Features

- SD device Controller Specifications version 2.00
- SDIO specifications version 2.00
- SD Physical Layer Specifications version 2.00
- Host clock rate 0 to 50 MHz
- Supports SPI, 1-bit and 4-bit SD modes
- Data rate up to 200 Mbps in 4-bit SD mode
- Support CRC7 and CRC16
- Supports IO52 and IO53 commands for SDIO cards
- Supports Read Wait Control and Suspend/Resume operations
- System Bus Interface – AHB

Functional Block Description

Host Registers

The registers block consists of fixed internal registers called Common IO Area (CIA). The registers within CIA are provided to enable/disable and control operation of IO functions. They also provide the capabilities and requirements of functions. The CIS0, CIS1 and CSA have to be implemented in CPU subsystem memory. They can be accessed through AHB master interface. These registers have read and write access from SD host and through AHB interface from the CPU.

Bus Interface Unit

The SDIO bus interface unit block communicates to the SD host through SD bus. It supports 1-bit, 4-bit SD and SPI modes. This block contains CRC7 and CRC16 generator & checker logic for CMD and DAT lines respectively. BIU converts the serial CMD and DAT lines to parallel. It converts byte aligned SD data to 32-bit interface to the FIFO for 1-bit, 4-bit SD and SPI modes. It also has the MUX logic for SPI and SD mode of operation.

Command Response SM

This state machines implements sending the commands out to SD interface according to device registers configuration and receives the response from the SD/SDIO devices. This state machine maintains the command response boundary on CMD line.

Data SM

This state machine is implemented to handle the data transfer to and from the DAT 0-3 lines in SPI, 1 and 4 bit SD modes.

FIFO

The SDIO device IP core has a 512x36 FIFO for communication between SD and AHB interfaces. A common buffer is used for reads and writes. The FIFO also stores byte enables for the DWORD. The IP has option of using Synchronous or Asynchronous DPRAMs.

Design Attributes

- Fully Synchronous Design
- Technology independent design
- Highly modular design
- Platforms : Solaris and Linux
- Verilog Simulators : Cadence NC-Verilog and Synopsys VCS
- FPGA Usage:
 - Device- Xilinx Spartan 3 xc3s1500
 - Slices Used – 2071
 - LUTs Used – 3277
 - RAMB16s Used – 2

Aizyc Advantage

- Scalable IP Core
- Compact Design
- Cost-effective
- Portability : ASIC, FPGA
- Validation on Xilinx Spartan 3
- Continuous support during integration, design and verification

Deliverables

- Synthesizable Verilog RTL
- Test bench and exhaustive Test cases
- Synthesis constraints and script files
- Sample AHB Slave Driver
- Documentation – User Manual, Verification plan , Validation Report, Synthesis, DFT and integration Guidelines



AHB slave

The AHB slave block is used to access the SD registers by the host CPU. It operates at AHB clock frequency and all the signals to/from this block are synchronized in SD clock domain. Simple AHB Read and Write commands are supported by the slave interface.

AHB Master DMA

The 32-bit AHB master interface is used to access the function specific registers and the memory. All data transfer commands to function 1 or accesses to CIS0, CIS1 and CSA are routed through AHB master interface.

Interrupt State Machine

This state machine implements the Interrupt timing control as per SDIO 2.0 specifications. The state machine supports optional Interrupt Period at the Data Block gap in 4-bit SD mode. It also implements the Read Wait Control logic by which the SD host can delay the Data Read from any function which is using the DATA lines.

Suspend/Resume Control

The suspend resume control logic implements the operation as per specifications. The SD host requests the lower priority or slower transactions to suspend using the DAT lines and restores later after completion of higher priority transactions.

Clock and Resets

This block generates all required clocks and resets for the IP core. It takes the asynchronous resets as input and generates resets synchronized to respective clocks in the design. This avoids the reset removal violations in the design. This block also has the clock switching circuit for FIFO control.

Contact Information

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