

## Overview

Aizyc SD/SDIO Host IP is compact low power and scalable IP core. It is easy to integrate and cost effective IP.

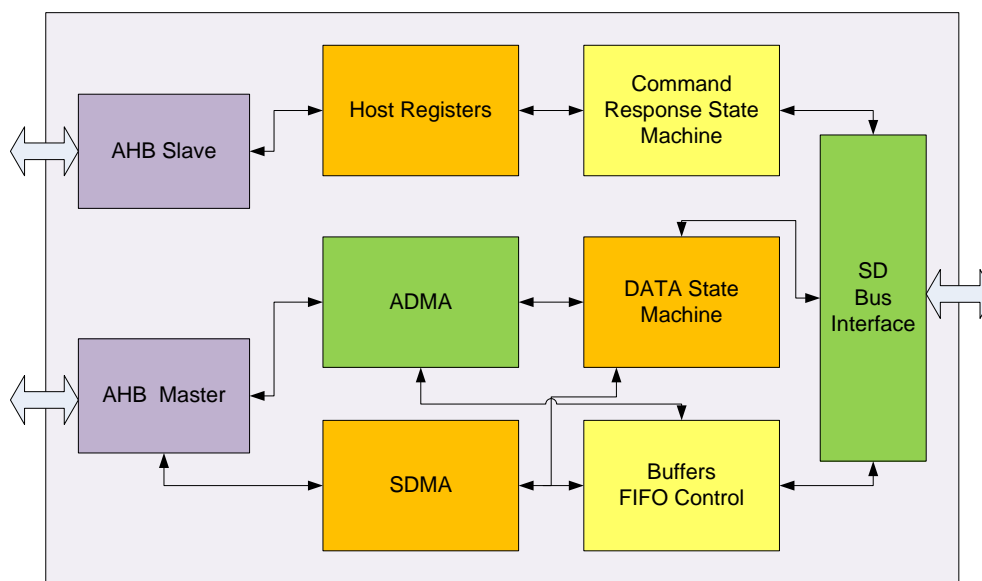
Aizyc's Host IP is fully compliant with the standard SD Host Controller Specifications Version 2.0, SDIO Specifications version 2.00 and SD Physical Layer Specifications Version 2.0. It supports SPI, 1-bit SD and 4-bits SD, high speed and full speed transfer modes. Data rate up to 200 Mbps in 4-bit SD mode is supported.

AHB Master & Slave interface in Host IP will allow easy integration in to SOC. The flexible architecture of the core will support wide range of applications – GPS , UWB, WiMAX etc.

The IP core is portable to an ASIC or a FPGA. It has been validated on Xilinx Spartan 3 platform.

Along with the IP core, we will provide complete test environment with constraint randomized test cases and our full support during integration.

## Functional Block Diagram



## SD/SDIO 2.0 – AHB Host IP

### Features

- SD Host Controller Specifications version 2.00
- SDIO specifications version 2.00
- SD Physical Layer Specifications version 2.00
- Host clock rate 0 to 50 MHz
- Supports SPI, 1-bit and 4-bit SD modes
- Data rate up to 200 Mbps in 4-bit SD mode
- Support CRC7 and CRC16
- Supports IO52 and IO53 commands for SDIO cards
- Supports Read Wait Control and Suspend/Resume operations
- System Bus Interface – AHB
- Optional Bus Interface – APB, OCP, VCI

## Functional Block Description

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### Host Registers

The registers block consists of standard host registers as per SD Host Controller Specification 2.00. These registers are used to control the function of host controller IP and are programmable through 32bit AHB slave interface.

### AHB Master/Slave Interface

The AHB slave interface is used to program the host registers. The 32 bits AHB master interface is used by SDMA and ADMA blocks to transfer data to and from system memory.

### Bus Interface Unit

The SD bus interface unit block communicates to the SD Device through SD bus. This block contains CRC7 and CRC 16 generator and checker logic for CMD and DAT lines respectively. BIU converts serial CMD and DAT lines to parallel.

### Command Response SM

This state machines implements sending the commands out to SD interface according to host registers configuration and receives the response from the SD/SDIO devices. This state machine maintains the command response boundary on CMD line.

### Data SM

This state machine is implemented to handle the data transfer to and from the DAT 0-3 lines in SPI, 1 and 4 bit SD modes.

### SDMA/ADMA

The DMA blocks implement the SDMA and ADMA interface respectively as mentioned in SD Host Controller Specs to transfer data to and from the system memory through AHB Master interface.

## Contact Information

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## Design Attributes

- Fully Synchronous Design
- Technology independent design
- Highly modular design
- Platforms : Solaris and Linux
- Verilog Simulators : Cadence NC-Verilog and Synopsys VCS
- FPGA Usage:
  - Device- Xilinx Spartan 3 xc3s1500
  - Slices Used – 2071
  - LUTs Used – 3277
  - RAMB16s Used – 2

## Aizyc Advantage

- Scalable IP Core
- Compact Design
- Cost-effective
- Portability : ASIC, FPGA
- Validation on Xilinx Spartan 3
- Continuous support during integration, design and verification

## Deliverables

- Synthesizable Verilog RTL
- Test bench and exhaustive Test cases
- Synthesis constraints and script files
- Sample AHB Slave Driver
- Documentation – User Manual, Verification plan , Validation Report, Synthesis, DFT and integration Guidelines