

Overview

Aizyc UART IP is compact low power and scalable IP core.

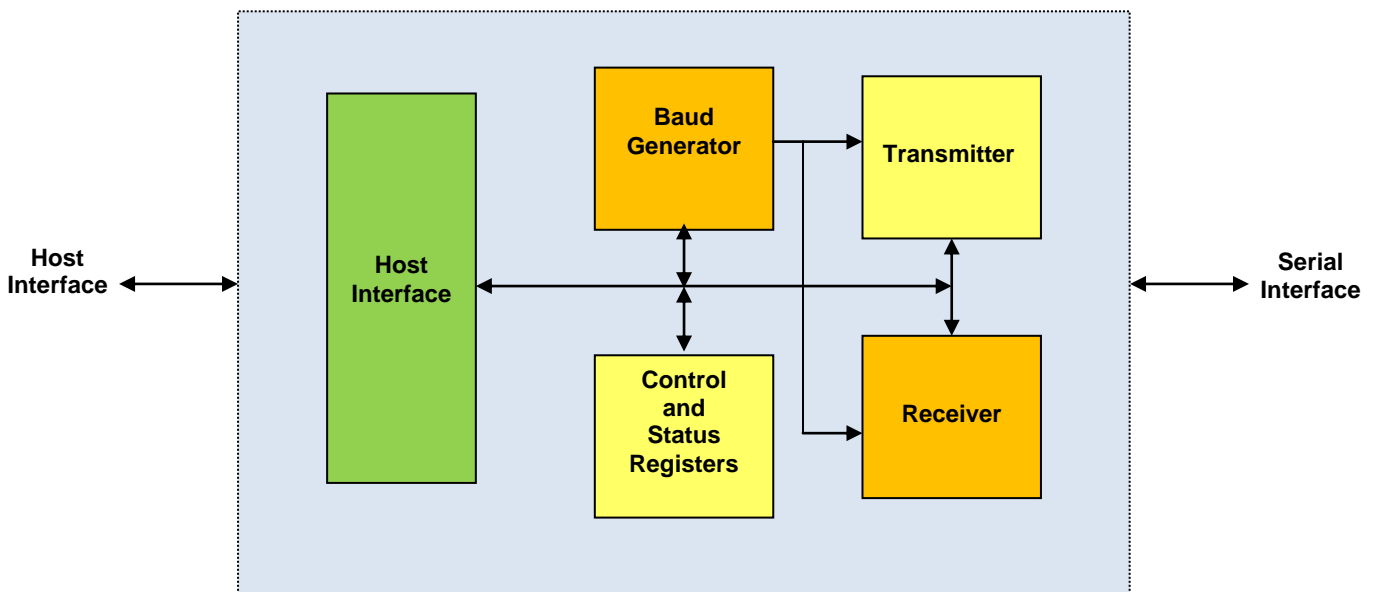
High performance Aizyc UART IP core is compliant to 16C450 and 16C550 Universal Asynchronous Receiver/Transmitter. This IP has deep FIFOs to achieve higher performance and throughput.

The Standard VCI (Virtual Component Interface) bus interface provided with the core makes integration easy into any design.

The IP core is portable to an ASIC or a FPGA. It has been validated on Xilinx platform.

Along with the IP core, we will provide complete test environment with constraint randomized test cases and our full support during integration.

Functional Block Diagram



UART IP

Features

- 16C450/16C550 compatible UART
- System Bus Interface – VCI
- Optional Bus Interface – AHB, APB, OCP
- Supports RS232 modes
- Bi-directional Speeds configurable from 50 bps to 115200 bps
- Full Serial modem control
- Supports Hardware as well as Software flow control
- 5, 6, 7, 8 bit serial format support
- Even, Odd, None, Space & Mark parity supported
- Transmit/Receive FIFO
- Status report capability

Functional Block Description

Host Interface

The host interface is a 32 bit VCI slave interface. This interface is used to integrate the IP core within the SoC design and to read/ write the internal registers of the core.

Baud Generator

This block generates the baud clock for transmitting and receiving the serial data based on the values programmed in the registers.

Control and Status Registers

This block consists of standard UART registers for data transfer and control and status information.

Transmitter

This block collects the parallel data coming from the host interface, accumulate it and transfer the data on the serial line according to RS232 protocol.

Receiver

This block collects the serial data coming on the serial input, accumulate it and transfer the data to the host interface in the parallel form.

Contact Information

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Design Attributes

- Fully Synchronous Design
- Technology independent design
- Highly modular design
- Platforms : Solaris and Linux
- Verilog Simulators : Cadence NC-Verilog and Synopsys VCS

Aizyc Advantage

- Scalable IP Core
- Compact Design
- Cost-effective
- Portability : ASIC, FPGA
- Validation on Xilinx
- Continuous support during integration, design and verification

Deliverables

- Synthesizable Verilog Source Code
- Test bench and exhaustive Test cases
- Synthesis constraints and script files
- Reference Device Driver for software development
- Documentation – User Manual, Verification plan , Validation Report, Synthesis, DFT and integration

Guidelines