

## Overview

Aizyc USB 2.0 Device Controller IP is compact low power and scalable IP core.

USB2.0 device controller IP core is fully synthesizable core suitable for different process. Generic application interface for easy integration. It supports different endpoint configurations for varied applications.

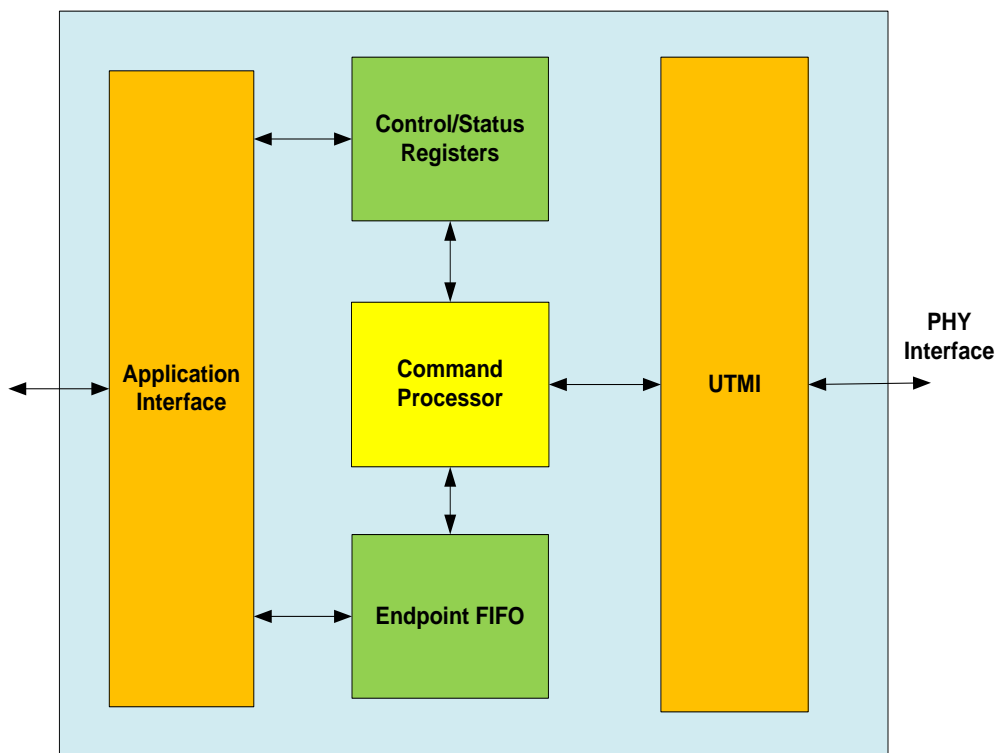
The IP core is portable to an ASIC or a FPGA. It has been validated on Xilinx platform. Along with the IP core, we will provide complete test environment with constraint randomized test cases and our full support during integration.

## USB 2.0 – Device Controller IP

### Features

- Fully compliant with USB Specification rev 2.0
- System Bus Interface – VCI
- Optional Bus Interface – AHB, APB, OCP
- Supports high (480 Mbps), full (12 Mbps) speed operation
- Supports Control, Bulk and Interrupt transactions
- External application interface
- Interface to support external UTMI PHY
- Customize endpoint numbers and configurations

## Functional Block Diagram





## Functional Block Description

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### Command Processor

The command processor is the important block of device controller. It does the decoding and execution of all standard commands. It also maintains the device state machine and the handshake database for standard and vendor specific commands.

### Control Endpoint

Endpoint controller has the control of all USB control transfers. It maintains the state machine for Setup, Data and Status stages of control transfers. Data toggle and handshakes for control transfers will be controlled in this module.

### Endpoint FIFO

Every endpoint in the device controller has associated FIFO buffer for data transfer. The buffer size for each endpoint is configurable.

### Application Interface

The device controller has a generic application interface which can be used to interface different applications. E.g. Ethernet, serial port, parallel port

### UTMI+/ULPI Interface

This interface is provided for external standard ULPI/UTMI+ PHY. This ULPI interface is a wrapper around UTMI+ interface. Any of the two interfaces can be used for external USB PHY

## Contact Information

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Aizyc Technology Private Limited  
6th Floor, Plot No: 488 & 489,  
Ayyappa Society, Madhapur  
(4th Left from Meridian School)  
Hyderabad - 500081, AP, India  
Phone: +91 40 6459 -9771, 6459-9770  
Email : sales@aizyc.com

USA Branch: 228 Hamilton ave,  
3rd Floor, Palo Alto, CA 94301  
Phone: +1 (408) 338 - 6929  
www.aizyc.com

### Design Attributes

- Fully Synchronous Design
- Technology independent design
- Highly modular design
- Platforms : Solaris and Linux
- Verilog Simulators : Cadence NC-Verilog and Synopsys VCS

### Aizyc Advantage

- Scalable IP Core
- Compact Design
- Cost-effective
- Portability : ASIC, FPGA
- Validation on Xilinx
- Continuous support during integration, design and verification

### Deliverables

- Synthesizable Verilog Source Code
- Test bench and exhaustive Test cases
- Synthesis constraints and script files
- Reference Device Driver for software development
- Documentation – User Manual, Verification plan , Validation Report, Synthesis, DFT and integration Guidelines